

REMARKS

This is in response to the Office Action dated October 24, 2003. New claims 12-14 have been added. Thus, claims 1-5 and 10-14 are now pending.

Claim 1

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Ball in view of Kitazawa and Sim. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 1 as amended requires "the region for forming the wiring layers for connecting adjacent functional blocks includes a coaxial line comprising an inner signal line for transmitting the signal of high frequency of several GHz or more, and an outer ground line surrounding the signal line via an insulating film as viewed cross sectionally, so that the inner signal line and outer ground line have a common axis along at least a portion of a length of the coaxial line, and wherein the region for forming the plurality of functional blocks and the region for forming the wiring layers for connecting adjacent functional blocks are each formed on a semiconductor substrate." In other words, *both the region for forming the claimed wiring layers and the region for forming the plurality of functional blocks are each formed on a single semiconductor substrate.*

Ball fails to disclose or suggest the aforesaid underlined and quoted aspect of claim 1. Ball relates to a technique for shielding a signal line provided *between* a plurality of IC chips. Thus, Ball clearly fails to disclose or suggest both the region for forming the claimed wiring layers and the region for forming the plurality of functional

blocks each being formed on a single semiconductor substrate such as in a single IC chip. Ball is entirely unrelated to the invention of claim 1 in this respect. Citation to the other art cannot overcome the aforesaid fundamental flaw of Ball. Thus, even if the art was combined as alleged in the Office Action (which would be incorrect in any event), the invention of claim 1 still would not be met.

Claims 3, 5

Claims 3 and 5 also require that both the region for forming the claimed wiring layers and the region for forming the plurality of functional blocks are each formed on a single semiconductor substrate. As explained above, the cited art fails to disclose or suggest this aspect of claims 3 and 5 either taken alone or in combination.

Claims 5, 10 and 11

The rejection of claim 5 is incorrect for yet another reason. Claim 5 requires that the wiring layers for connecting the functional blocks includes wiring layers thicker than those in the functional blocks. For example, see Figs. 10-11 where the wiring layer(s) for connecting the functional blocks (see Figs. 10(B-3) and 11(B-5)) are thicker than the wiring of the functional blocks (see Figs. 10(A-3) and 11(A-5)). None of the three (3) cited references disclose or suggest this "thicker" aspect of claim 5. The Examiner's allegation that it would have been obvious to use thicker wiring layers in the connection area than in the functional blocks is unsupported since no cited reference discloses or suggests such a feature.

The rejections of claims 10-11 is flawed in a similar manner. In particular, the cited art fails to disclose or suggest the "thickness greater" aspect of claims 10-11.

Furthermore, the combination of Parikh with Ball and Kitazawa is legally incorrect. In particular, Parikh relates to a triple damascene structure; and Ball/Kitazawa do not. Moreover, Parikh never puts one line above or below another line; this is in direct contrast with Ball and Kitazawa. Thus, Parikh is not properly combinable with Ball or Kitazawa. The Section 103(a) rejection of claim 5 is fatally flawed for this additional reason.

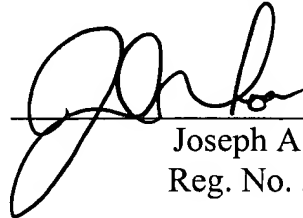
Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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